SWITCHING OF MRAM DEVICES HAVING SOFT MAGNETIC REFERENCE LAYERS

Field of the Invention

[0001] The present invention relates to magnetic memory devices, and more specifically to techniques for switching of the memory devices.

Background of the Invention

[0002] Non-volatile memory devices such as magneticrandom access memory (MRAM) devices are of interest for replacement of volatile memory devices such as dynamic random access memory (DRAM) devices. Such MRAM devices include an array of individual MRAM cells which may be tunnelling magnetoresistance memory (TMR) cells, colossal magnetoresistance memory cells (CMR) or giant magnetoresistance memory (GMR) cells.

[0003] In general, the MRAM cells include a data layer and a reference layer. The data layer is composed of a magnetic material and during a write operation the magnetisation of the data layer can be switched between two opposing states by an applied magnetic field and thus binary information can be stored. The reference layer usually is composed of a magnetic material in which the magnetisation is pinned so that the magnetic field that is applied to the data layer and in part penetrates the reference layer, is of insufficient strength to switch the magnetisation in the reference layer.

[0004] For example in a TMR cell the data layer and the reference layer are separated by a thin dielectric layer which is arranged so that a tunnelling junction is formed. Any material comprises two types of electrons which have spin-up and spin down polarity. In the case of

a ferromagnetic layer that has a magnetization, more electron spins have one orientation compared with the other one which gives rise to the magnetization. The electrical resistance through the layers is dependent on the relative orientations of the magnetizations in the data and reference layers. This is the tunneling magneto-resistance (TMR) effect and the state of the data layer can be read by measuring the apparent electric resistance across the layers.

[0005] The data layer typically includes a low coercivity material that can be switched in its magnetic direction by column and row data-write currents.

[0006] The reference layer usually is fabricated with a high coercitivity material and is permanently magnetized in a set direction during an annealing processing step.

[0007] In one version of the memory cell, namely the so-called the "spin-valve", the reference layer is "pinned" by exchange coupling by an adjacent antiferromagnetic layer.

[0008] Alternatively, the reference layer may be soft-magnetic reference layer and may have a lower coercivity so that the reference layer may be switched together with the data layer. In this case the magnetic field of a control current is used to switch the magnetization of the reference layer to the reference state after the data layer is switched. The coercivity of the reference layer and the magnitude of the control current need to be chosen so that switching the reference layer does not affect the data layer.

[0009] In general, the magnetic memory cells should be as small as possible. However, the smaller the cells are made, the more sensitive they are to thermal stability problems during operation. In order to compensate, the

small magnetic memory cell data layer are fabricated with magnetic material that is more resistant to magnetic change. Unfortunately, generating the stronger fields necessary makes switching the memory cells more difficult during the write operation. Hence, there is a need for a magnetic memory device in which writing is facilitated.

Summary of the Invention

[0010] Briefly, a magnetic random access memory (MRAM) embodiment of the present invention includes an array of magnetic memory cells. A plurality of word and bit lines connects columns and rows of the memory cells so that the memory cells are positioned at cross-points of the word and bit lines. Each memory cell has a magnetic reference layer and a magnetic data layer. Each magnetic reference layer and each magnetic data layer has a magnetization that is switchable between two states under the influence of a magnetic field and each reference layer has at a first temperature a coercivity that is lower than that of each data layer at the first temperature. The MRAM also includes a plurality of heating elements each proximate to a respective data layer. Each heating element provides in use for localized heating of the respective data layer to reduce the coercivity of the data layer so as to facilitate switching of the data layer.

[0011] The present invention will be more fully understood from the following description of specific embodiments. The description is provided with reference to the accompanying drawings.

Brief Description of the Drawings

[0012] Fig. 1 is a perspective diagram of a magnetic memory device according to a specific embodiment;

[0013] Fig. 2 is a schematic cross-sectional diagram of a magnetic memory device according to another specific embodiment;

[0014] Fig. 3 is a schematic cross-sectional diagram of a magnetic memory device according to a further specific embodiment and

[0015] Fig. 4 is a schematic diagram of a computer system embodying the device shown in Figure 1; and

[0016] Fig. 5 is a flow-chart for a method embodiment.

Detailed Description

[0017] Fig. 1 represents a magnetic random access memory (MRAM) array according to a specific embodiment, and is referred to herein by the general reference numeral 100. The MRAM 100 includes an array of magnetic memory cells 102 and electrical heaters 103 in a cross-point arrangement. In this embodiment, each memory cell 102 is based on tunneling magneto-resistance (TMR) technology in which tunneling currents tunnel through a dielectric layer affected by local magnetic fields. Individual cells 102 are selectively addressed for read-write access by word lines 104 and 106, and bit lines 108. These word and bit lines represent hundreds of such lines that constitute and implement the cross-point array.

[0018] When a data-write current is applied to bit line 108, a magnetic field will surround the bit line. The magnetic field is used to switch the magnetic memory cells 102 by switching the permanent-magnet data layer to

the opposite polarization. Binary information can therefore be stored as a function of the direction of the magnetic field generated by the current applied to bit line 108. During switching the heaters 103 generate heat which lowers the magnetic field strength that is required to switch the memory cells 102 and thus heating facilitate switching of the memory cells.

[0019] Fig. 1 includes a data-write generator 110 that outputs a data-write current through bit line 108. The circuit may also generate a current through word lines 104 and 106. (Electrical connections to the data-write generator 110 are not shown for word lines 104 and 106).

[0020] Although not illustrated in Fig. 1, MRAM 100 typically includes a read circuit for sensing the resistance of selected memory cells 102. During read operation, a constant voltage is applied to the bit line 110 and sensed by the read circuit. An external circuit may provide the constant supply voltage.

[0021] MRAM 100 may comprise an array having any number of memory cells 102 arranged in any number of rows and columns. It can also use alternative technologies such as colossal magneto-resistance memory cells (CMR), and giant magneto-resistance memory (GMR) cells.

[0022] Fig. 2 shows a cross-sectional diagram of the memory cell 202 contacted by the word line 204. The memory cell 202 comprises a data layer 208, a thin dielectric layer 210 and a reference layer 212. In general, MRAM 200 is such that the magnetization in the data layer 208 can have two opposing directions so that binary information can be stored as a function of the direction of the magnetic field generated by the current applied to bit line 216.

[0023] The data layer 208 uses a magnetic material

with a direction of magnetization that can be switched as a function of an applied magnetic field. The reference layer 212 is a soft magnetic layer and has a coercivity that is lower than that of the data layer 208. When the magnetization of the data layer 208 is switched, the magnetization of the soft-magnetic reference layer 212 typically will also switch. After a switching operation a current will be directed through word line 204 so that a magnetic field is generated in the reference layer 212 that will ensure that the magnetization of the reference layer has a predetermined direction and the layer can therefore function as a reference layer. The control current is selected so that the magnetization of the data layer, having a higher coercivity, is not affected.

[0024] The thin dielectric layer 210 is thin enough so that a tunneling current will flow through the dielectric layer when a suitable electrical potential is applied. The tunneling probability, and therefore the impedance of the memory cell, depends on the direction of the magnetization in the data layer 212 relative to that of the reference layer 208. Therefore, it is possible to determine the orientation of the magnetization in the data layer from the tunneling current which is dependent on the resistance of the memory cell 102.

[0025] In this embodiment a further layer 214 is positioned between the data-layer 208 and the bit line 216. Layer 214 may be a dielectric layer so that, when a potential is applied between the word line 204 and the bit line 216 a tunneling current will flow through the dielectric layer 214 which will result in the generation of heat. Alternatively, layer 214 may be a resistive layer composed of a material that has a relatively low electrical conductivity and heat may be generated

resistively without a tunneling current. In any case, the generated heat diffuses at least in part into the data layer 208. Owing to the heat the magnetic field strength required to switch the magnetization of the data layer 208 is lower and thus heating of the data layer 208 facilitates switching of the magnetization.

[0026] Typically further layers are positioned between the data layer 208 and the bit line 216 which are not shown in order to improve clarity. For example, the layer 214 may be separated by one or more of these layer from the data layer 208 and/or the bit line 216.

[0027] If the layer 214 is a dielectric layer through which in use a tunneling current passes, the layer 214 may have a thickness ranging from 0.5nm to 10nm and may be composed of any suitable dielectric material including for example aluminum oxide (Al_2O_3), aluminum nitride (AlN), silicon oxide (SiO_2), silicon nitride (Si_3N_4), boron nitride (BN), Magnesium oxide (MgO), tantalum oxide (Ta_2O_5, or in general TaO_x) and many others. In this example the layer has a thickness of 2nm and a planar area of 130 x 260nm.

[0028] If the layer 214 is a resistive layer it may be composed of any suitable resistive material including semiconductors (e.g., Si, Ge, Se, graphite (Carbon), SiC), some conductive oxides (e.g. TaO_2), silicides (e.g., WSi, CoSi, FeSi, PtSi), nitrides (e.g., TaN, FeAlN, SiN). In the case of this variation of the embodiment, the layer 214 is composed of SiC. In this example the layer 214 has an area of approximately 130 x 260nm and a thickness of about 5nm.

[0029] In this particular example the data layer 208 is composed of nickel iron (NiFe), the reference layer 212 is in this example a thin ferro-magnetic layer and

composed of NiFe. The dielectric layer 210 is composed of Al_2O_3. All layers have the same planar area of approximately 130nm x 260nm, and the reference layer 212, the data layer 208 and the dielectric layer 210 have a thickness of approximately 2nm, 4nm, and 2nm, respectively. The resistance of the layers 210 and 214 are approximately the same. Therefore, the device comprises two heat sources that develop approximately the same amount of heat. The word and bit lines are composed of copper.

[0030] Fig. 3 shows a cross-sectional representation of a portion of device 300. An electrical heater is positioned in the proximity of the magnetic memory cell 302 and in this embodiment the electrical heater is a thin film diode 304. Diode 304 is sandwiched between bit line 306 and memory cell 302. The memory cell 302 comprises data layer 308, dielectric layer 310 and reference layer 312. As for MRAM 200 shown in Fig. 2 and discussed above, the reference layer 312 is a soft magnetic layer and has a coercivity that is lower than that of the data layer 308.

[0031] Typically further layers are positioned between the data layer 308 and the bit line 306 which are not shown in order to improve clarity. For example, the diode 304 may be separated by one or more of these layer from the data layer 308 and/or the bit line 306.

[0032] The magnetic memory cell 302 is contacted by word line 314. When a potential is applied between the word line 314 and the bit line 306 a current will flow through the diode 304 which will result in the generation of resistive heat. The resistance of the diode 304 and therefore the heat that is generated depends on the operating conditions. For example, when the diode is reverse biased, the resistance will be relatively high

whereas the resistance is lower when the diode is forward biased.

[0033] The device 300 is similar to the device 200 shown in Fig. 2. The data layer 308 is composed of nickel iron (NiFe), the reference layer 312 is a soft magnetic reference layer and is composed of NiFe and the dielectric layers 310 is composed of Al_2O_3. All layers have the same planar area of approximately 130nm x 260nm, and the reference layer 312, the data layer 308 and the dielectric layer 310 have a thickness of approximately 2nm, 4nm, and 2nm, respectively.

[0034] The diode 304 diode may be a conventional p-n junction and may also be a metal-semiconductor (Schottky diode) such as Pt-Si diode. The diode 304 may be incorporated into the substrate (ie into a silicon substrate). In this embodiment, the diode 304 is made with single-crystal silicon and is fabricated in the substrate level. An alternative fabrication procedure involves making an amorphous-silicon based diode. In this case the silicon can be deposited by using PECVD, CVD techniques as a thin layer within the multiple metal layers of the MRAM cell. This is particularly advantageous as then the MRAM cell can be integrated at the upper levels of the interconnects (Copper levels) in a CMOS process.

[0035] As device 100 shown in Fig. 1, devices 200 and 300 typically include read circuits for sensing the resistance of selected memory cells. During read operation, a constant voltage is applied to the bit lines and sensed by the read circuit. An external circuit may provide the constant supply voltage.

[0036] MRAMs 200 and 300 may comprise an array having any number of memory cells arranged in any number of rows and columns. They can also use alternative technologies

such as colossal magneto-resistance memory cells (CMR), and giant magneto-resistance memory (GMR) cells.

[0037] Fig. 4 shows a computer system 400 which embodies the memory device shown in Figure 1. The computer system 400 has a main board 402 which is connected to a central processing unit 404 and magnetic memory device 406. The magnetic memory device arrays 406 includes the device shown in Fig. 1. The magnetic memory device array 406 and the central processing unit 404 are connected to a common bus 408. The computer system 404 has a range of further components which are for clarity not shown.

[0038] Fig. 5 illustrates a method embodiment for operating an MRAM device. The method 500 comprises step 502 of heating MRM cells, such as those shown in Fig. 1. The method 500 includes step 504 of utilizing the generated heat to facilitate cell state switching.

[0039] Although the invention has been described with reference to particular examples, it will be appreciated by those skilled in the art that the invention may be embodied in many other forms. For example, the MRAM device may comprise more than one electrical heater for each MRAM cell. In addition, further layers may be disposed between the memory cell and the at least one electrical heater or between the at least one electrical heater and the bit line. In this case the magnetic memory cell may be electrically isolated form the bit and/or word lines. For example, a sense conductor may be in electrical contact with the memory cell (ie with the data layer) and an electrically insulating layer may be disposed between the bit line and the sense layer. Further, it will be appreciated that each magnetic memory cell may comprise a

number of additional layers such as capping, AF and seed layers.

[0040] In addition the soft reference layer of each memory cell may include a respective word line. For example, a conductive core may carry the read and control currents. The core may be cladded with a ferromagnetic material that has a low coercivity. If the MRAM device comprises TMR cells, the cladded core may be positioned adjacent the dielectric layer of a respective TMR cell so that a current may tunnel between the cladding and the data layer through the dielectric layer.